REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on September 25, 2001, and the references cited therewith. No claims are amended, no claims are canceled, and no claims are added; as a result, claims 26-39 are now pending in this application.

Miscellaneous

The Applicant respectfully requests the Examiner to note that a Supplemental Preliminary Amendment (in addition to a Supplemental Information Disclosure Statement) in this matter was filed after filing the instant application, before the mailing date of the Office Action. These circumstances were called to the attention of the Examiner in telephone messages and a teleconference held on October 24, 2001. The Examiner said he would check with "someone else" to determine whether the Supplemental Preliminary Amendment was too burdensome to consider. However, the Applicant was never informed as to whether any further action would be taken, and to the best of Applicant's representative's knowledge, no Supplemental Office Action has been mailed. As a courtesy, Exhibit A, attached hereto, includes a copy of the Supplemental Preliminary Amendment, filed on September 19, 2001.

The Applicant notes the Examiner's request for submission of a priority statement to change the priority date. The Applicant supplies the statement as part of the amendments to the specification text, above.

§102 Rejection of the Claims

Claims 26, 29, 32 and 35-39 were rejected under 35 USC § 102(a) as being anticipated by "Intel" Electronic News, (EN) December 5, 1994 in view of 82430FX PCIset Datasheet 80437FX System Controller (TSC) and 82438FX Data Path unit (TDP), Intel Corp., pp 1-67, 11/96 (INTEL). The Applicant respectfully traverses this rejection.

The Office Action, under MPEP §§ 2124 and 2131.01, asserts that the EN reference discloses the invention as claimed by the Applicant. The INTEL reference, published after the priority date of the present application, is used to allege that some of the elements claimed by the Applicant are inherent in the computer system described by the EN reference. However, simply accumulating a collection of elements does not guarantee their structure or operation is the same as the invention claimed by the Applicant.

As noted in a previous Office Action response, MPEP §2112 sets forth the standard for reliance on inherency:

> In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the inherent characteristic necessarily flows from the teachings of the applied prior art. *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter., 1990) (emphasis in original).

The Applicant respectfully asserts that the Examiner has not met this standard. The EN reference merely discloses the existence of the Triton chip set. EN does not disclose burst mode memory, while each one of the currently pending claims specifically includes the element of "burst EDO" memory, as well as the ability to *direct memory controller operations based on data read from the memory devices*. While the device discussed in EN may operate using the EDO mode or Page mode, there is no evidence that the device disclosed by EN will operate with burst mode memories. There is also no evidence whatsoever that the Triton chip set disclosed by EN in fact contained each and every element described in INTEL at the time of the EN reference publication.

The Applicant respectfully requests identification of specific sections in INTEL which support this particular rejection, as well as direct evidence that the chip set discussed in EN is necessarily identical to that described in the INTEL reference. The only response given in the Office Action with respect to such specificity is that INTEL "discloses a burst mode" on page 1. In reality, INTEL discloses a mode called "pipelined fast page mode", which requires two /CAS cycles for every read operation, and actually takes longer than conventional page mode. The term "burst" is never used. Since the citation to INTEL in the Office Action does not teach, or even suggest, burst operation, INTEL can not be used to read into EN that which INTEL does not teach.

Still further, the M.P.E.P. requires that "[t]he identical invention must be shown in as complete detail as is contained in the ... claim." *See* M.P.E.P. § 2131. The Office Action fails to demonstrate how the element "a processor ... responsive to ... information from the memory to program the memory controller to provide a set of access control signals ... in accordance with the memory device mode, wherein the information ... includes data read from the memory device." is disclosed by the EN reference. Thus, the EN reference (which, due to priority, is the only reference that can be used to reject the claims under 35 USC § 102(a)) is also deficient in this respect.

Accordingly, under the guidance of M.P.E.P. §2112, INTEL is not determinative of inherency with respect to each and every element of the invention, since there is no evidence to support identical devices between the EN and INTEL references, nor with respect to disclosing true burst mode memory operation. In addition, the EN reference fails to disclose every element of the invention, as claimed. In view of the foregoing, Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 26, 29, 32, and 35-39 under 35 U.S.C. §102(a).

§103 Rejection of the Claims

Claims 27-28, 30-31, 33 and 34 were rejected under 35 USC § 103(a) as being anticipated by "Intel" Electronic News, (EN) December 5, 1994 in view of 82430FX PCIset Datasheet 82437FX System Controller (TSC) and 82438FX Data Path Unit (TDP), Intel Corp., pp. 1-67, 11/96 (INTEL) and further in view of Fung et al. (Fung) US Patent No. 5,630,163. The Applicant respectfully traverses the Examiner's rejection of these claims.

To establish a prima facie case of obviousness, the references themselves must provide a suggestion or motivation for combination. M.P.E.P. § 2143.01. References must be considered in their entirety, including parts that teach away from the claims. MPEP 2141.02. "One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed Cir., 1988). In this case, the combined teachings of the references are not the same as that claimed by the Applicant, and can not be combined to operate as such.

As noted in a previous response by the Applicant, Fung et al. completely fails to teach or even suggest detecting memory device modes of operation. Fung at al. merely speaks to determining the memory *size*. The only citation offered in the Office Action (Fung, column 1, lines 25-32) also fails to go beyond this teaching, and does not answer the prior request by the Applicant to cite the text of Fung et al. which speaks to detecting the memory device *mode* of operation. As such, Fung et al. can not be used to supply the deficiencies of the EN reference. Combining Fung et al. with the EN reference produces a system which is inoperative to detect the mode of the memory devices contained therein. Further, the INTEL reference is predated by the instant application priority filing date, and it is therefor improper to combine INTEL with the EN reference with respect to rejection of the claims under 35 USC § 103(a). Thus, claims 27-28, 30-31, and 33-34 should be in condition for allowance, due to the deficiencies of Fung et al. and INTEL.

Claims 26, 29, 32 and 35-39 were rejected under 35 USC § 103(a) as being anticipated by Farrer et al. (US Patent No. 5,307,320) in view of Micron, "Reduce DRAM cycle times with Extended Data-Out", Micron technical Note pp 5-33 thru 5-40, 4/94 and further in view of Wyland (US Patent No. 5,261,064). The Applicant respectfully traverses the Examiner's rejection of these claims.

After noting that Farrer et al. fails to disclose a memory including EDO and fast page mode elements, as claimed by the Applicant, it is asserted in the Office Action that Micron can be combined with Farrer et al. to supply these missing elements to provide a functional system which operates to detect memory modes and then programs the memory controller accordingly. The Applicant respectfully requests the Examiner to note that Farrer et al., as well as Micron, fail completely to provide a processor which responds to information (including data read from the memory device) to program the memory controller for the provision of memory access signals, as claimed by the Applicant.

In addition, the Office Action fails to cite a credible suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art (supported by some reference, and not a bare assertion), to modify any of the cited references in a manner necessary to support the rejection. For example, it is asserted that Micron allows

"design of the computer system [based?] on the type of memory that offers the target price/performance ration [sic] of the system." However, this goes against the entire premise of the Applicant's invention. There is no need to design the computer for a particular memory type, since several types can be accommodated by the *same* processor, controller, bus, etc. It is hardly advantageous to redesign an entire computer system to accommodate various memory types; such remarks are quite confusing with respect to the meaning intended by the Office Action language.

After admitting that neither Ferrer et al. and the Micron references disclose a burst mode of operation, a similar situation arises with the assertion that "Wyland discloses [a] burst mode of operation ... in order to increase access time." And that it would be obvious to combine Wyland and Ferrer for the purpose of "... increasing access time thereby increasing overall system performance." Why would one wish to increase access time, when this actually decreases memory access performance? For these reasons, the Applicant urges again that the burden of establishing a *prima facie* case of obviousness has not been met in the Office Action, requests clarification of these confusing and contradictory remarks, and respectfully requests reconsideration and withdrawal of the Examiner's rejection of Claims 26, 29, 32 and 35-39 under 35 USC § 103(a) as being anticipated by Farrer, Micron, and Wyland.

Claims 27-28, 30-31, and 33-34 have been rejected under 35 USC § 103(a) as being anticipated by Farrer et al., Micron, Micron technical Note pp 5-33 thru 5-40, 4/94 and Wyland US Patent No. 5,261,064 and further in view of Fung et al (Fung) US Patent No. 5,630,163. The Applicant respectfully traverses the Examiner's rejection of these claims.

As noted previously, the admitted defects of Farrer et al., Wyland, and the Micron references to anticipate a power-up detection circuit of the type claimed by the Applicant can not possibly be remedied by the inclusion of Fung et al. Fung et al., which completely fails to teach or even suggest detecting memory device modes of operation.

Fung at al. merely speaks to determining the memory *size* upon the application of power. The only citation offered in the Office Action (Fung, column 1, lines 25-32) also fails to go beyond this teaching, and does not answer the prior request by the Applicant to cite the text of Fung et al. which speaks to detecting the memory device *mode* of operation. As such, Fung et al.

can not be used to supply the deficiencies of the Ferrer et al., Wyland, and Micron references. In fact, as noted above, combining Fung et al. with Ferrer et al., Wyland, and the Micron references provides a system which is inoperative to detect the mode of the memory devices contained therein.

Further, considering the arguments set forth by the Applicant previously, and combining the deficiencies in the references noted by the Examiner, the Applicant respectfully urges that no credible motivation to combine Farrer, the Micron references, Wyland, and Fung et al. so as to support a rejection of these claims based on obviousness, as required by the M.P.E.P. Stating that "it is immaterial that [a] reference does not disclose specific function[s] set forth in Applicant's specification" is logically flawed. There is ample precedent to establish that functional limitations are appropriate in claims and should be afforded patentable weight. For example, see In re Ludtke, 169 U.S.P.Q. 563, 566 (CCPA 1971) and In re Land, 151 U.S.P.Q. 621 (CCPA 1966). Therefore, the Applicant respectfully requests reconsideration by the Examiner with respect to the admitted deficiencies in the references.

None of the cited references demonstrates the use of burst memory in combination with the other claimed elements of the invention. As noted above, and pursuant to MPEP § 2144.03, the Applicant requests that the Examiner provide a specific reference supporting the alleged facts. In the absence of such a specific reference, the Applicant asserts that the Examiner has not met the burden of establishing a *prima facie* case of obviousness, and requests reconsideration and withdrawal of the rejection of claims 27-28, 30-31, 33 and 34 under 35 USC § 103(a) as being anticipated by Farrer et al., Wyland, the Micron references,and Fung et al.

Conclusion

The Applicant has reviewed the other art made of record in the Office Action, but does not believe it is more pertinent than the cited art. The Applicant respectfully submits that all of the pending claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612-373-6904) to facilitate prosecution of this application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

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Respectfully submitted,

BRETT L. WILLIAMS

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6913

Date 11/30/2001 By

Edward J. Brooks, III
Reg. No. 40,925

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 30th day of November 2001.

Name Amy Moriarty

Signature